

AMENDMENTS TO THE CLAIMS

Claims pending

- At time of the Action: Claims 1-32.
- After this Response: Claims 1, 3-9, 12, 16-21, 23, 25, 26 and 29-47.

Canceled or Withdrawn claims: 2, 10, 11, 13-15, 22, 24, 27 and 28.

Amended claims: 1, 3, 8, 12, 17-21, 23, 25 and 26.

New claims: 33-47.

1. (Currently Amended) A method comprising:

creating mappings from ~~a logical~~received ~~addresses space~~ to physical memory by a hardware interface disposed between a processor and a number of physical memory devices; and

~~identifying portions of the logical address space based on usage;~~

modifying the mappings by the hardware interface to reduce the number of physical memory devices that are targeted by the mappings; ~~and~~

~~receiving memory instructions that reference memory in terms of the logical address space.~~

2. (Cancelled)

3. (Currently Amended) A memory controller comprising:

means for receiving memory instructions from a processor that specifies memory addresses ~~that reference memory~~ in terms of a logical address space;

1 means for identifying portions of the logical address space based on usage;
2 and
3 means for mapping the identified portions of the logical address space to
4 physical memory in a manner that reduces the number of physical memory devices
5 referenced by the identified portions of the logical address space .
6

7 4. (Original) A memory controller as recited in claim 3, wherein the means for
8 identifying include means for monitoring the memory instructions to determine
9 more frequently used portions of the logical address space.
10

11 5. (Original) A memory controller as recited in claim 3, wherein the means for
12 identifying include means for monitoring the memory instructions to determine
13 more recently used portions of the logical address space.
14

15 6. (Original) A memory controller as recited in claim 3, wherein the means for
16 identifying include means for receiving notifications regarding logical memory
17 allocations and de-allocations.
18

19 7. (Original) A memory controller as recited in claim 3, wherein the means for
20 identifying include means for receiving notifications regarding actual usage of
21 logical memory addresses.
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1 8. (Currently Amended) A memory controller as recited in claim 3, wherein the
2 means for identifying action include means for maintaining one or more in-use
3 registers indicating whether corresponding portions of physical memory are
4 currently in use.

5
6 9. (Original) A memory controller as recited in claim 3, further comprising:
7 means for identifying one or more memory devices that are not referenced
8 by the identified portions of the logical address space; and
9 means for setting said one or more identified memory devices to a reduced
10 power mode.

11
12 10-11. (Canceled)

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14 12. (Currently Amended) A memory controller as recited in claim 3, further
15 comprising:

16 means for identifying one or more physical memory areas that are relatively
17 infrequently referenced by the identified portions of the logical address space; and
18 means for setting said one or more physical memory areas to a reduced
19 power mode.

20
21 13-15. (Canceled).

1 16. (Original) A memory controller as recited in claim 3, further comprising:

2 a means for periodically repeating the identifying and mapping actions to
3 repeatedly reduce the number of physical memory devices referenced by the
4 identified portions of the logical address space; and

5 means for moving affected portions of physical memory so that each
6 logical address continues to reference the same data prior to any repeated mapping
7 action.

8
9 17. (Currently Amended) A method of managing memory, comprising:

10 monitoring memory accesses received from a processor to identify portions
11 of a ~~logical~~the processor's address space based on usage; and

12 periodically re-mapping the ~~logical-processor's~~ address space to physical
13 memory to reduce the number of physical memory devices referenced by the
14 identified portions of the ~~logical-processor's~~ address space.

15
16 18. (Currently Amended) A method as recited in claim 17, wherein the
17 monitoring comprises monitoring the memory instructions to determine more
18 frequently used portions of the ~~logical-processor's~~ address space.

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20 19. (Currently Amended) A method as recited in claim 17, further wherein the
21 monitoring comprises monitoring the memory instructions to determine more
22 recently used portions of the ~~logical-processor's~~ address space.

1 20. (Currently Amended) A method as recited in claim 17, further comprising:
2 receiving memory instructions that reference memory in terms of the
3 ~~logical-processor's~~ address space; and
4 monitoring the memory instructions to identify the portions of the ~~logical~~
5 ~~processors~~ address space..
6

7 21. (Currently Amended) A method as recited in claim 17, wherein the identified
8 portions of the ~~logical-processor's~~ address space are those portions that are used
9 least frequently, further comprising:

10 identifying one or more memory devices that are not referenced by the
11 identified portions of the ~~logical-processor's~~ address space; and

12 setting said one or more identified memory devices to a reduced power
13 mode.
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15 22. (Canceled).
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17 23. (Currently Amended) A method as recited in claim 17, wherein the identified
18 portions of the ~~logical-processor's~~ address space are those portions that are used
19 least frequently, further comprising:

20 identifying one or more physical memory areas that are not referenced by
21 the identified portions of the ~~logical-processor's~~ address space; and

22 setting said one or more physical memory areas to a reduced power mode.
23

24 24. (Canceled).
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1 25. (Currently Amended) A method as recited in claim 17, further comprising:
2 prior to any re-mapping action, moving affected portion of physical
3 memory so that ~~each logical addresses~~ received from the processor continues to
4 reference the same data.

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6 26. (Currently Amended) A system comprising:

7 ~~a plurality of physical memory devices containing physical memory;~~
8 ~~a memory controller configured to reference the physical memory in~~
9 ~~response to received memory instructions specifying addresses in terms of a~~
10 ~~logical address space;~~

11 an operating system configured to dynamically allocate memory from ~~the a~~
12 logical address space and to identify allocated portions of the logical address space
13 to ~~the a~~ memory controller;

14 the operating system further configured to dynamically de-allocate memory
15 from the logical address space and to identify the de-allocated portions of the
16 logical address space to the memory controller;

17 wherein the memory controller is configured to ~~respond to the operating~~
18 ~~system by mapping map~~ allocated portions of the logical address space to
19 corresponding portions of physical address space ~~memory~~ in a manner that tends
20 to reduce the number of physical memory devices referenced by the allocated
21 portions of the logical address space; and

22 the memory controller further configured to move portions of memory
23 regions corresponding to allocated portions of the logical address space in
24 response to identification of de-allocated portions of the logical address space and
25 re-mapping the corresponding portions of the physical address space and

1 corresponding portion of the logical address space to reduce the number of
2 physical memory devices referenced by allocated portion of logical memory.

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4 27-28. (Canceled).

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6 29. (Original) A memory management system comprising:

7 means for maintaining a free region list indicating free memory regions for
8 potential allocation from physical memory devices;

9 means for sorting the free region list in an order that is based on the relative
10 current allocations of memory regions from respective sets of one or more
11 physical memory devices; and

12 means for allocating memory regions indicated by the sorted free region list
13 on the sorted order so that the memory regions are allocated preferentially from
14 those physical memory devices having higher relative current allocations of
15 memory regions.

16
17 30. (Original) A memory management system as recited in claim 29, further
18 comprising:

19 means for identifying one or more memory devices having relatively lower
20 current allocations of memory regions; and

21 means for setting said one or more identified physical memory devices to a
22 reduced power mode.

1 31. (Original) A memory management system as recited in claim 29, further
2 comprising means for maintaining the free region list as a linked list of free region
3 indicators.

4
5 32. (Original) A memory management system as recited in claim 29, further
6 comprising means for repeatedly re-sorting the free region list in said order.

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8 33. (New) The system as recited in Claim 26, further comprising:
9 identifying one or more of a plurality of memory devices having relatively
10 lower allocated portions of memory regions; and
11 setting the identified one or more of the plurality of memory devices to a
12 reduced power state.

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14 34. (New) The system as recited in Claim 26, further comprising:
15 identifying one or more of the plurality of memory devices based on
16 relatively lower usage; and
17 setting the identified one or more of the plurality of memory devices to a
18 reduced power state.

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20 35. (New) The system as recited in Claim 34, wherein identifying one or more of
21 the plurality of memory device based on relatively lower usage comprises
22 monitoring memory instructions to determine relatively less frequently used
23 portions of the physical address space.

1 36. (New) The system as recited in Claim 34, wherein identifying one or more of
2 the plurality of memory device based on relatively lower usage comprises
3 monitoring memory instructions to determine relatively least recently used
4 portions of the physical address space.

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6 37. (New) The memory controller as recited in claim 3, wherein the means for
7 identifying include means for identifying portions of the processor's physical
8 address space based on frequency of usage.

9
10 38. (New) The memory controller as recited in claim 3, wherein the means for
11 identifying include means for identifying portions of the processor's physical
12 address space based on most recent usage.

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14 39. (New) The method as recited in Claim 1, further comprising receiving
15 memory instructions from a processor or graphics adapter by the hardware
16 interface.

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18 40. (New) The method as recited in Claim 1, wherein the mappings are modified
19 at the hardware interface independently of the operating system.

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21 41. (New) The method as recited in Claim 1, further comprising refreshing the
22 content of physical memory devices by the hardware interface independently of
23 the operation system

24
25 42. (New) The method as recited in Claim 1, further comprising:

1 identifying one or more of the plurality of memory devices referenced by
2 relatively few mappings; and

3 setting the identified one or more of the plurality of memory devices to a
4 reduced power state.

5
6 43. (New) The method as recited in Claim 1, wherein the received addresses are
7 specified by a processor in terms of a physical address space, further comprising:

8 identifying portions of the processor's physical address space based on
9 usage;

10 re-mapping the identified portions of the processor's physical address space
11 to physical memory by the hardware interface in a manner that reduces the number
12 of physical memory devices referenced by the identified portions of the
13 processor's physical address space; and

14 prior to re-mapping, moving the corresponding memory content so that the
15 corresponding memory content will continue to be referenced by the same
16 received address.

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18 44. (New) The method as recited in Claim 43, wherein the re-mapping is
19 periodically performed after a pre-defined number of memory references.

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21 45. (New) The method as recited in Claim 43, wherein the re-mapping is
22 performed after power consumption by the physical memory reaches a determined
23 threshold.

1 46. (New) The method as recited in Claim 43, wherein the re-mapping is
2 periodically performed after a pre-defined number of memory allocations.

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4 47. (New) The method as recited in Claim 43, wherein the re-mapping is
5 performed at periodic time intervals.
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